Course Structure & Curriculum

for

M. Tech. Programme

in

Electronics Engineering

with specialization in

Microelectronics and VLSI Design

Department of Electronics and Communication Engineering

Motilal Nehru National Institute of Technology Allahabad

Allahabad - 211004, Uttar Pradesh

MOTILAL NEHRU NATIONAL INSTITUTE OF TECHNOLOGY ALLAHABAD

VISION

To establish a unique identity for the Institute amongst National and International Academic and Research Organizations through knowledge creation, acquisition and dissemination for the benefit of Society and Humanity.

MISSION

To generate high quality human and knowledge resources in our core areas of competence and in emerging areas to make valuable contribution in technology for social and economic development of the Nation and to make organized efforts for identification, monitoring and control of objective attributes of quality for continuous enhancement of academic processes, infrastructure and ambiance.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To become a globally leading department of higher learning, building upon the culture, the values of universal science and contemporary education, and a center of research and education generating the knowledge and the technologies which lay the groundwork in shaping the future in the fields of Electronics and Communication Engineering.

MISSION

To provide quality education and research leading to B. Tech., M. Tech. and Ph. D. degree in the area of Electronics and Communication Engineering and Technology which may produce globally acceptable high quality skilled manpower.

To impart technical education which may provide innovative skills in their respective area of specialization for society in general with universal moral values, adherent to the professional ethical codes.

To generate and disseminate knowledge and technologies essential to the local and global needs in the field of Electronics and Communication Engineering.

M.Tech. (Electronics Engineering)

with specialization in Microelectronics and VLSI Design

Course Structure & Scheme of Evaluation I Semester

Subject Code	Subject Name	L	T	P	Credits				Total Marks
						TA	MSE	ESE	
EC21101	Semiconductor Devices and Modelling	3	1	0	4	20	20	60	**100**
EC21102	Digital IC Design	3	1	0	4	20	20	60	**100**
EC213xx	Elective I	3	1	0	4	20	20	60	**100**
EC213xx	Elective II	3	1	0	4	20	20	60	**100**
EC212xx	Elective III	0	0	6	4	50	-	50	**100**

Total Credits = 20

II Semester

Subject Code	Subject Name	L	T	P	Credits				Total Marks
						TA	MSE	ESE	
EC22101	VLSI Technology and Process Modelling	3	1	0	4	20	20	60	**100**
EC22102	VLSI Circuits and Systems	3	1	0	4	20	20	60	**100**
EC223xx	Elective IV	3	1	0	4	20	20	60	**100**
EC223xx	Elective V	3	1	0	4	20	20	60	**100**
EC222xx	Elective VI	0	0	6	4	50	-	50	**100**

Total Credits = 20

III Semester

Subject Code	Subject Name	Credits	Eval (100)
EC23601	Thesis	16	Marks
EC23651	Special Study/Industrial Training/Colloquium	4	Marks

Total Credits = 20

IV Semester

Subject Code	Subject Name	Credits	Eval (100)
EC24601	Thesis	20	Marks

Total Credits = 20

Note: The distribution of thesis evaluation marks will be as follows:

1. Supervisor(s) evaluation component 60%
2. Oral Board evaluation component 40%

List of Professional Electives for Microelectronics and VLSI Design

Elective I (EC213xx)

1. EC21301 Analog IC Design
2. EC21302 VLSI CAD
3. EC21303 System on Chip
4. EC21304 VLSI for Telecommunications
5. EC21305 MEMS and Integrated Sensors

Elective II (EC213xx)

1. EC21306 Digital Signal Processing
2. EC21307 Nanoelectronic Devices and Engineering
3. EC21308 Reconfigurable Hardware Design
4. EC21309 Architectural Design of ICs
5. EC21310 VLSI for Signal Processing

Elective III (EC212xx)

1. EC21201 System Design using HDL
2. EC21202 Simulation Lab - I
3. EC21203 Digital Signal Processing Lab

Elective IV (EC223xx)

1. EC22301 Advanced Analog Design
2. EC22302 Compound Semiconductor and Applications
3. EC22303 Mixed System IC Design
4. EC22304 Low Power VLSI Design
5. EC22305 RF IC Design

Elective V (EC223xx)

1. EC22306 Embedded Systems
2. EC22307 Mixed Mode Signal Processing
3. EC22308 ASIC Design
4. EC22309 VLSI Testing and Testable Design

Elective VI (EC222xx)

1. EC22201 FPGA / CPLD Lab
2. EC22202 Analog IC and Digital IC Design Lab
3. EC22203 Simulation Lab - II

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO 1	To excel in professional career and/or higher education by acquiring knowledge in area of Microelectronics and VLSI Design
PEO 2	To analyze real time problems, design appropriate system to provide solutions that are technically sound, economically feasible and socially acceptable
PEO 3	To exhibit professionalism, ethical attitude, communication skills, team work in their profession and adapt to current trends by engaging in lifelong learning

Mapping of Mission statements with the PEOs

Key components from Department Mission	**PEO 1**	**PEO 2**	**PEO 3**
To provide quality education and research leading to B. Tech., M. Tech. and Ph. D. degree in the area of Electronics and Communication Engineering and Technology which may produce globally acceptable high quality skilled technical manpower To impart technical education which may provide innovative skills in their respective area of specialization for society in general with universal moral values, adherent to the professional ethical codes To generate and disseminate knowledge and technologies essential to the local and global needs in the field of Electronics and Communication Engineering			
Quality education	YES		
Professional career	YES	YES	YES
Higher education	YES	YES	
Social responsibility			YES
Research		YES	

EC21101 Semiconductor Devices and Modelling **FIRST SEMESTER**

Introduction & review of Diodes and Transistor (BJT) modelling, semiconductor surfaces, ideal MOS, real/non-ideal MOS, band diagrams, 2-terminal MOS, 3-terminal MOS, MOS as a capacitor, C-V characteristics, flat-band, threshold voltage, electrostatics of a MOSC, mobility, MOSFET, I-V characteristics, scaling, short channel and narrow channel effects-high field effects, MOS transistor in dynamic operation, large signal modeling, small signal model for low, medium and high frequencies, SOI devices, Multi-gate SOI MOSFETs, alternate MOS structures.

References:

1. B. G. Streetman, *Solid State Electronics Devices*, Prentice Hall, 2002
2. Y. Taur, T.H.Ning, *Fundamentals of Modern VLSI Devices*, Oxford
3. Yannis Tsividis, Colin McAndrew, *Operation and Modelling of the MOS Transistor*, Oxford, Third Edition
4. James B. Kuo and Ker-Wei Su, *CMOS VLSI Engineering Silicon-on-Insulator (SOI)*, Springer
5. Jean-Pierre Colinge, *FinFETs and Other Multi-Gate Transistors*, Springer 2007
6. S.M. Kang and Y. Leblevici, *CMOS Digital Integrated Circuits Analysis and Design*, TMH,Third edition
7. Behzad Razzavi, *Microelectronics*

EC21102 Digital IC Design **FIRST SEMESTER**

Basic electrical properties of MOS circuits: MOS transistor operation in linear and saturated regions, MOS transistor threshold voltage, MOS switch and inverter, latch-up in CMOS inverter; sheet resistance and area capacitances of layers, wiring capacitances, CMOS inverter properties - robustness, dynamic performance, regenerative property, inverter delay times, switching power dissipation, cross talk, combinational logic design in CMOS. MOSFET scaling - constant-voltage and constant-field scaling, Dynamic CMOS design: steady-state behavior of dynamic gate circuits, noise considerations in dynamic design, charge sharing, cascading dynamic gates, domino logic, NP-CMOS logic, problems in singlephase clocking, two-phase non-overlapping clocking scheme, Subsystem design: design of arithmetic building blocks like adders - static, dynamic, Manchester carry-chain, look-ahead, linear and square-

root carry-select, carry bypass and pipelined adders and multipliers, serialparallel Braun, Baugh-Wooley and systolic array multipliers, barrel and logarithmic shifters, area-time tradeoff, power consumption issues, designing semiconductor memory and array structures: memory core and memory peripheral circuitry, virtual and high speed memory design, custom cell based design, digital circuit testing and testability.

References:

1. J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits- A Design Perspective*
2. S. M. Kang and Y. Leblevici, *CMOS Digital Integrated Circuits Analysis and Design*
3. N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design - a System Perspective*
4. Mead and Convay, *Introduction to VLSI Systems*
5. W. Wolf, *Modern VLSI Design - System on Chip design*
6. R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*

EC22101 VLSI Technology and Process Modelling **SECOND SEMESTER**

Crystal growth & wafer preparation, Processing considerations: Chemical cleaning, gettering the thermal stress factors etc.

Epitaxy: Vapors phase epitaxy basic transport processes & reaction kinetics, doping & auto doping, equipments & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

Oxidation: Growth mechanism & kinetics, silicon oxidation model, interface considerations, orientation dependence of oxidation rates in thin oxides, oxidation techniques & systems, dry & wet oxidation, masking properties of SiO_2.

Diffusion: Diffusion from a chemical source in vapour form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer.

Lithography: Optical Lithography: optical resists, contact & proximity printing, projection printing, Electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X-ray sources & masks. Ion lithography.

Etching: Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced

etching, properties of etch processing. Reactive ion beam etching, specific etches processes: poly/polycide. Trench etching.

References:

1. S. M. Sze, *Modern Semiconductor Device Physics*, John Wiley & Sons, 2000
2. B.G. Streetman, *Solid State Electronics Devices*, Prentice Hall, 2002
3. Chen, *VLSI Technology*, Wiley, March 2003
4. S. K. Gandhi, *VLSI fabrication principles*
5. J. D. Plummer, Michael D. and Peter D. Griffin, *Silicon VLSI Technology: fundaments, practice and modelling*

EC22102 VLSI Circuits and Systems **SECOND SEMESTER**

Designing High-Speed CMOS Logic Networks: Gate delays, driving large capacitive loads, logical effort, optimizing number of stages, branching, BiCMOS drivers.

Advanced Techniques in CMOS Logic Circuits: Mirror circuits, Pseudo-nMOS, domino logic, adiabatic logic, tri-state circuits, clocked CMOS, dynamic CMOS logic Circuits, dualrail logic networks.

System Specifications using Verilog Codes: Basic concepts, structural, gate level modeling, switch level modeling, design hierarchies, behavioral, dataflow modeling and RTL.

General VLSI System Components using Verilog Codes: Multiplexers, binary decoders, equality detectors and comparators, priority encoder, shift and rotation operations, latches, D flip-flop, registers and their structural description using Verilog.

Arithmetic Circuits in CMOS VLSI using Verilog Codes: Bit adder circuits, ripple-carry adders, carry look-ahead adders, other high-speed adders, and their Verilog implementation, Booth algorithm and Booth encoded digit operations and array multipliers.

Reliability and Testing of VLSI Circuits: General concepts, reliability modeling and performance metrices, CMOS testing, test generation methods: logical effects of faults, the D-Algorithm, path sensitization and basic networks for deriving the boolean difference.

References:

1. Neil H. E. Weste and David M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley
2. John P. Uyemura, *Introduction to VLSI Circuits and Systems*, John Wiley & Sons, INC.
3. Neil H. E. Weste and Kamran Eshraghian, *Principles of CMOS VLSI Design*, Addison-Wesley, MA

EC21301 Analog IC Design **FIRST SEMESTER (E-I)**

Basic MOS Device Physics: A review, single-stage amplifiers, basic concepts, commonsource stage, types of load source follower, common-gate stage, cascode stage folded cascode. Differential amplifier - single-ended and differential operation, basic differential pair: quantitative and qualitative analysis, common-mode response differential pair with MOS loads, Gilbert cell.

Current mirrors and references, basic current mirrors, cascode current mirrors, advanced current mirrors, active current mirrors: large-signal and small-signal analysis, basic voltage and current references.

Operational amplifiers: performance parameters, one-stage Op-amps, two-stage Op-amps, current conveyer.

Operational transconductance amplifier, current feedback amplifier.

References:

1. Behzad Razavi, *Design of Analog CMOS Integrated Circuits*
2. Allen and Holberg, *CMOS Analog Circuit design*
3. Gray, Hurst, Lewis and Meyer, *Analysis and Design of Analog CMOS Integrated Circuits*

EC21302 VLSI CAD **FIRST SEMESTER (E-I)**

Hierarchical view of VLSI design, architectural design, high level synthesis, scheduling, data path synthesis, logic synthesis, minimization techniques, circuit design and simulation, layout synthesis, placement and routing, DRC, silicon compiler, array processors.

References:

1. M. Sarrafzadeh and C. K. Wong, *An introduction to physical design*, McGrew Hill
2. Naveed Sherwani, *Algorithm for VLSI Design Automation*, Springer
3. S. M. Sait and H. Youssef, *VLSI Physical design automation: theory and practice*, World Scientific Pub. Co.

EC21303 System on Chip **FIRST SEMESTER (E-I)**

Introduction to digital system and VLSI design, design techniques, fabrication processes and steps, wires and vias, design rules and layout. Logic gates, static complementary gates, nonconventional logic circuits, low power gate circuits, delay through interconnect. Combinational logic network, network delay, logic and interconnect design, power optimization and logic testing. Sequential machines, latches and flip-flops, clocking techniques, sequential system design, optimization, validation and testing.

Chip design: design methodologies, timing specifications, architecture design layout with validation, data paths.

References:

1. Wayne Wolf, *Modern VLSI Design*, Third Edition
2. Neil Weste, *Principles of CMOS VLSI Design*

EC21304 VLSI for Telecommunications **FIRST SEMESTER (E-I)**

Building blocks of signal processing systems, dedicated architectures, architecture of a transceiver, front end ICs for wireless systems, direct conversion receivers, processors for cellular telephony, chip sets for GSM and CDMA for various protocols, chipsets for satellite TV receiver, ICs for digital TV and image compression, ICs for fibre optic communication, ATM switching, ICs for error correction and detection.

References:

1. Y. Tsividis, P. Antognetti, *Design of MOS VLSI Circuits for Telecommunications,* Prentice-Hall
2. Bosco Leung, *VLSI for Wireless Communication,* 2nd Edition, Springer

EC21305 MEMS and Integrated Sensors **FIRST SEMESTER (E-I)**

Introduction to MEMS, MEMS technologies, applications, micromachining- surface and bulk, MEMS processes, principle of sensors, smart sensors, temperature sensors, pressure and strain gauges, optical sensors, PH sensors, on-chip integration of sensors, micropower Opamps, BIMOS chips for analog and digital functions, micromachined actuators, flow sensors, accelerometers, gyro, biomedical and process control chips with integrated sensors.

References:

1. Elena Gaura, *Smart MEMS and Sensor Systems*, Imperial College Press
2. James J. Allen, *Micro electro Mechanical System Design*, CRC Press
3. Vijay K. Vardan, K.J. Vinoyn and K. A. Jose, *RF MEMS and their Applications*, Wiley

EC21306 Digital Signal Processing **FIRST SEMESTER (E-II)**

Fundamentals of Digital Signal Processing: Review of signals and systems, DTFT and Z-Transform.

Discrete Fourier Transform (DFT): Sampling in frequency domain, DFT: properties of the DFT, computational aspect of DFT, circular and linear convolution using DFT, filtering of long data sequence.

FFT Algorithm: Decimation-in-time radix-2 FFT algorithm, decimation-in-frequency radix2 FFT algorithm, Goertzel algorithm.

Digital Filters and Finite Wordlength Effects: Basic structure of IIR and FIR systems, specifications of filters, pipelining and parallel processing of FIR filters, state variable representation of digital filter. Finite wordlength effects: parasitic oscillations, scaling of signal levels, round-off noise, measuring round-off noise, coefficient sensitivity, sensitivity and noise, effect of round off noise in digital filters.

Filter Design Techniques: Digital and analog filtering, filter specifications, magnitude and phase responses, IIR and FIR filters, design of IIR filter, impulse - invariant transformation, Bilinear Z-transform, design of FIR filters using impulse response truncation, FIR filter design using windows, effect of windowing, rectangular, Bartlett, Hanning, Hamming, Blackmann and Kaiser windows.

Multirate Digital Signal Processing: Fundamentals of multirate signal processing, sampling rate conversion, interpolation, decimation, noble identities, polyphase representations, filter banks and perfect reconstruction systems, multirate system advantages and applications.

Digital Signal Processors – Architectures, Implementations and Applications: Introduction, digital signal processors architectures, the TMS320 family, selection of processors, software developments, system considerations, implementation considerations, data representations and arithmetic, finite wordlength effects, programming issues, hardware interfacing, fixed-point and floating-point implementations.

Statistical Signal Processing: Power spectrum estimation of signals – Wide sense stationary random processes, power spectral density, non parametric methods – periodogram, Backman-Tuckey method, parametric method – ARMA, AR processes, Yule-Walker method.

References:

1. J. G. Proakis and D.G. Manolakis, *Digital Signal Processing: Principles, Algorithms and Applications*, Pearson Education
2. A. V. Oppenheim, *Applications of Digital Signal Processing*
3. A. V. Oppenheim, A. S Willsky, and S. H. Nawab, *Signals and Systems*, PrenticeHall, Englewood Clieffs
4. K. K. Parhi, *VLSI Digital Signal Processing Systems- Design and Implementation*, John Wiley & Sons
5. Sanjit K. Mitra, *Digital Signal Processing: A Computer based approach*, McGraw Hill, 1998
6. Sen M. Kuo and Woon-Seng Gan, *Digital Signal Processors, architectures, implementations and applications*, Prentice-Hall
7. V. Madisetti, *The Digital Signal Processing Handbook*, IEEE press, ISBN 0849385725
8. R. E. Crochiere and L. R. Rabiner, *Multirate Digital Signal Processing*, PrenticeHall, 1983

EC21307 Nanoelectronic Devices and Engineering **FIRST SEMESTER (E-II)**

Shrinking of device dimensions from micrometres to nanometres, limitations of conventional devices, quantum mechanics of nanometric structures, concept of quantum wells, quantum wires and quantum dots, fundamentals of carrier transport in quantum structures, temperature effects, MODFETs, HBTs and other ultra-high-performance devices for future ULSI, super lattices, resonant tunneling phenomena, opto-electronic interactions in quantum structures, quantum lasers, single-carrier devices, formation of quantum structures, element of nanoelectronic device processing.

References:

1. Paul Harrison, *Quantum wells, wires and dots: Theoretical and Computational Physics of Semiconductor Nanostructures*, Second Edition, Wiley-Interscience
2. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Oxford

3. S. M. Sze, *Physics of Semiconductor Devices*, Wiley
4. Yannis Tsividis, Colin McAndrew, *Operation and Modelling of the MOS Transistor*, Oxford, Third Edition
5. B. G. Streetman, *Solid State Electronics Devices*, Prentice Hall
6. Mark Lundstrom, Jing Guo, *Nanoscale Transistor Device Physics, Modeling and Simulation*, Springer
7. Mark Lundstrom, *Fundamentals of carrier transport*, Cambridge
8. Jean-Pierre Colinge, *FinFETs and Other Multi-Gate Transistors*, Springer 2007

EC21308 Reconfigurable Hardware Design **FIRST SEMESTER (E-II)**

Introduction to reconfigurable design, objectives, advantages and performance issues, classification/types of reconfigurability, details of logic reconfiguration, instruction set reconfiguration, static vs dynamic reconfiguration, full or partial reconfiguration, fine grained, medium grained and coarse grained reconfiguration. Hardware vs software configurability and reconfigurability. Flow of reconfigurable design including synthesis, program execution and reconfigurable processor, reconfigurable instruction cell array. Algorithms related to different design steps of reconfigurable architecture. Fault covering problem in reconfigurable VLSI, fault covers in heterogeneous and general arrays. Fault diagnosis in reconfigurable VLSI and WSI processors arrays. Reconfigurable architecture design for different applications including DSP and Communication. Testability for reconfigurable VLSI architecture. Network on Chips (NOC).

References:

1. P. -E. Gaillardon, *Reconfigurable Logic: Architecture, Tools, and Applications,* CRC Press
2. John V. Oldfield and Richard C. Dorf, *Field-Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems,* Wiley Pub
3. Scott Hauck and André DeHon, *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation*

EC21309 Architectural Design of ICs **FIRST SEMESTER (E-II)**

Introduction, general design methodologies, datapath synthesis, mapping algorithms into architectures, control strategies, concepts of system analysis, hardware implementation of various control structures, microprogram control techniques, implementation of simple and nested subroutine calls, timing considerations, worst case system speed calculation, pipelined and parallel architectures, latency and throughput, dependency and dataflow, fault tolerance, fault-tolerant architectures.

References:

1. Sajjan G. Shiva, *Computer Organization, Design and Architecture*, 5th edition, CRC Press Taylor and Fransis group
2. Sung Kyu Lim, *Design for High Performance Low Power and Reliable 3D Integrated Circuits*, Springer

EC21310 VLSI for Signal Processing **FIRST SEMESTER (E-II)**

VLSI implementation and design issues related to discrete fourier transform, digital filter design techniques, computation of discrete fourier transform, discrete Hilbert transform, discrete random signals, effect of finite register length in digital signal processing, homomorphic signal processing, power spectrum estimation. Design issues related to VLSI for signal processing.

References:

1. Jose Epifanio Franca and Yannis Tsividis, *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, Second Edition, Prentice Hall
2. Keshab K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, First Edition, Wiley-Interscience
3. Richard J. Higgins, *Digital signal processing in VLSI*, Prentice Hall

EC21201 System Design using HDL **FIRST SEMESTER (E-III)**

List of Experiments:

1. Design and simulation of half-adder and full-adder using different modeling
2. Design and simulation of half-subtractor and full-subtractor
3. Design and simulation of 4-bit parallel adder
4. Design and simulation of full adder using half-adder

5. Design and simulation of 4:1 multiplexer
6. Design and simulation of 16:1 multiplexer using 4:1 multiplexer
7. Design and simulation of 3:8 decoder
8. Design and simulation of D, T, SR, JK & Master-slave Flip-flops
9. Design and simulation of Ring and Johnson counter
10. Design and simulation of up, down, up/down counter
11. Design and simulation of universal shift-register
12. Design and simulation of 3-bit Gray counter
13. Design and simulate given problem
14. Design and simulate sequence detector
15. Draw the state diagram, state table of given circuit
16. Design and simulate the sequence detector given in state diagram
17. Design and simulate mod-3 counting with half duty cycle

EC21202 Simulation Lab - 1 **FIRST SEMESTER (E-III)**

List of experiments:

1. Write a hardware description of 4-bit adder and subtractor and test their operations
2. Write a hardware description of degree to radian convertor
3. Write a hardware description of 4-bit mod-13 counter and test its operation
4. Write a hardware description of 8-bit register with shift left and shift right and test its operation
5. Write a hardware description of 4-bit array multiplier
6. Write a hardware description of 4-bit Booth multiplier
7. Design NOT, NOR, NAND gates using MENTOR GRAPHICS and compute the delay between input and output waveforms
8. Design 2:1 MUX using MENTOR GRAPHICS and compute the delay between input and output waveforms
9. Design XOR, NOR and NAND gates with CMOS and pseudo nMOS techniques using MENTOR GRAPHICS and compute the delay between input and output waveforms and compare them
10. Design XNOR gate using CMOS and pseudo nMOS techniques using MENTOR GRAPHICS and compute the delay between input and output waveforms and compare them
11. Design and simulate D-Flip Flop as a master-slave configuration using MENTOR GRAPHICS
12. Design and simulate ring oscillator using MENTOR GRAPHICS
13. Design 2:1 MUX using transmission gate and simulate using MENTOR GRAPHICS
14. Design and simulate 6T SRAM using MENTOR GRAPHICS

EC21203 Digital Signal Processing Lab **FRST SEMESTER (E-III)**

List of experiments:

1. Write a Matlab program to generate the following sequence.
   a) Unit sample sequence [$\delta(n)$].
   b) Unit step sequence [$u(n)-u(n-m)$].
   c) Unit ramp sequence
   d) Sine wave
   e) Cosine wave
2. Write a Matlab program to generate an exponential sequence.

   $X(n)=(a)^n \quad for \quad (a)\,0\le a\le 1 \quad (b)\,-1\le a\le 0 \quad (c)\,a\le -1 \quad (d)\,a>1$
3. Write a Matlab program to generate the signal S(n) = 2 * n * (0.8^ n)

   corrupted by the noise d(n) resulting the signal X(n). X (n) = s (n) +d (n)

   Also down sample the corrupted signal
4. Generate a Gaussian number with mean = 20 and variance = 40. Also plot the PDF of generated number
5. Generate Gaussian number with mean = 0 and variance = 1. Plot the generated number and calculate 3rd moment i.e. skewness using

$$\text{Skew}(X_1, X_2, ..., X_n) = \frac{1}{N}\sum_{j=0}^{1}\left[\frac{Xj - mean}{\sigma}\right]\text{^}3$$

6. Plot the following expressions for $H(z)$ in Z-plane

   a) $\dfrac{2Z^{-1}+9Z^{-2}+18^{-3}+48^{-4}}{3Z^{-1}+3Z^{-2}+15Z^{-3}-12Z^{-4}}$

   b) $\dfrac{5Z^{-1}-9Z^{-2}+16Z^{-3}-14Z^{-4}}{Z^{-1}-2Z^{-2}+10Z^{-3}-4Z^{-4}+64Z^{-5}}$

7. Determine the factor form of following Z-transforms

a) $G(z) = \dfrac{2Z^4 + 7Z^3 + 48Z^2 + 56Z}{32Z^4 + 3Z^3 - 15Z^2 + 18Z - 12}$

b) $G(z) = \dfrac{4Z^4 - 9Z^3 + 15Z^2 - 7}{Z^4 - 2Z^3 + 10Z^2 + 6Z + 64}$

8. Plot the following functions:

h(n)={4rn cos[pi*n(1+r)/m]+m sin[pi*n(1-r)/m]}/[1-4rn/m)^2]*pi*nm

h (0)=(1/m)+(r/(m * 4/pi -1))

h (|m/4|)=(-r/m)*[(2*cos{(pi/4*r)*(1+4)}-cos{pi*(1-r)/4*r}]

Given: m = 4, r = 0.1

9. A LTI system is given by

$$y(n) + 0.75y(n-1) - 0.48y(n-2) - 0.9y(n-3) = 0.58x(n) + 0.95x(n-1) + 0.49x(n-2) + x(n-3)$$

Write the program to compute and plot the impulse response of the system

10. Write a program to compute M-point DFT of following N-point sequence

$$x(n) = \begin{cases} n & 0 <= n <= N-1 \\ 0 & otherwise \end{cases}$$

Assume N = 16 and M = 32

11. Write a program to compute M-point IDFT of following N- point sequence

$$X(k) = \begin{cases} k/N & 0 < k < N-1 \\ 0 & otherwise \end{cases}$$

Assume N = 16 and M = 32

12. Write a MATLAB program to develop a signal y(n) generated by a convolution of two sequences x(n) and h(n). Also verify the result using in-built functions

13. Generate Gaussian distributed numbers and uniformly distributed numbers and find the correlation between them

14. Write a Matlab program to perform circular convolution of two finite unequal length sequences

15. Design a FIR lowpass filter with given specifications and verify the magnitude, phase, impulse response using FDA toolbox.

Order = 100

Window = Rectangular window

Cut off frequency in radian/sec = 0.4

16. Design a IIR lowpass Butterworth filter with following specifications and verify magnitude, phase, impulse response using FDA toolbox.

    Order Minimum

    Pass Band attenuation in dB: 0.36

    Stop Band attenuation in dB: 36

    Pass Band frequency in Hz: 1500

    Stop Band frequency in Hz: 2000

    Sampling frequency in Hz: 6000

17. Design the following circuits using simulink tool box on Matlab
    a) Half adder and Full adder
    b) Half wave rectifier and Full wave bridge rectifier
18. Design the following circuits using simulink tool box on Matlab
    a) Amplitude modulation and demodulation
    b) Frequency modulation and demodulation
19. Write a program to read a RGB image and perform the following operations on the image
    a) Extract Red, Green and Blue components of the image and then combine them to get the original image
    b) Convert the RGB image into Grey Scale image
    c) Resize the image to 512 X 512
    d) Add and subtract another RGB image to the original image.
    e) Calculate the sizes of all the images
20. Write a program to read a RGB image and perform the following operations on the image:
    a) Calculate the discrete cosine transform of the image and then recover the original image
    b) Add Gaussian noise to gray scale image and then recover the original gray scale image
21. Plot Sine and Cosine waves using TMS-320C6713
22. Find the Linear convolution of any two sequences and plot the output using TMS-320C6713

EC22301 Advanced Analog Design **SECOND SEMESTER (E-IV)**

Noise analysis, frequency response and its compensation, stability in analog circuits. Review of classical Op-amp, high performance CMOS Op-amp, discrete-time signals, introduction to switched capacitor circuits, frequency synthesizers, oscillators and phase locked-loop. comparators, Data converters: fundamentals, D/A and A/D converter, continuous time filter.

References:

1. B. Razavi, *Design of CMOS VLSI Design*
2. D. A. Johns and K. Martin, *Analog Integrated Circuit Design*
3. P. R. Gray and R. G. Meyer, *Analysis and design of Analog Integrated circuits* 4. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*

EC22302 Compound Semiconductor and Applications **SECOND SEMESTER (E-IV)**

Compound semiconductor classifications, an introduction to bulk compound semiconductor crystal growth, electronic properties of compound semiconductor materials, photonic applications of compound semiconductor materials, optoelectronic sources and detectors, semiconductor lasers, avalanche photodiode, high speed device applications - HEMT, MESFET, DC and AC analysis, equivalent circuits, frequency response etc., MISFETs, high speed logic circuits using GaAs MESFET and HEMTs, microwave and millimeter wave sources, Gunn diodes, applications of compound semiconductors as sensors and actuators.

References:

1. Tho T. Vu, *Compound Semiconductor Integrated Circuits*, World Scientific

EC22303 Mixed System IC Design **SECOND SEMESTER (E-IV)**

Review of CMOS process, device modelling, passive components and their parasitics, MOS transistor large and small signal modelling, CMOS amplifier basics, gain and bandwidth, cascode stages, differential amplifier, device matching considerations - current and voltage sources, current mirrors, simple voltage references, bandgap voltage reference. CMOS operational amplifiers, stability considerations and dominant-pole compensation, fully differential amplifiers, dynamically biased amplifiers. Data conversion circuits, basic requirements, simple voltage and current scaling D/A, comparators, integrating A/D, charge redistribution A/D, flash A/D, sigma-delta ADC and DAC, switched capacitor techniques,

resistor equivalent, stray insensitive integrators, Biquad design continuous time filters, OTA, clock generation for mixed signal system ICs, g_m-C Filter CFA and its applications, digital PLL circuits.

References:

1. Armin Tajalli, Yusuf Leblebici, *Extreme Low Power mixed Singal IC design,* Springer
2. M. Fakhfakh, E. T. Cuautle, R. C. Lopez, *Analog RF and Mixed Signal Circuit Systematic Design,* Springer

EC22304 Low power VLSI Design **SECOND SEMESTER (E-IV)**

Need for low power VLSI chips, sources of power dissipation on digital integrated circuits. Emerging low power approaches. Physics of power dissipation in CMOS devices. Device & technology impact on low power. Dynamic dissipation in CMOS, transistor sizing & gate oxide thickness, impact of technology scaling, technology & device innovation. Power estimation.

Simulation power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte-Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy, low power design.

Circuit level: Power consumption in circuits, Flip-Flops & Latches design, high capacitance nodes, low power digital cells library.

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Low power architecture & systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power clock distribution: Power dissipation in clock distribution, single driver vs distributed buffers, zero skew vs tolerable skew, chip & package co-design technique of clock network.

Algorithm & architectural level methodologies: Introduction, design flow, algorithmic level analysis & optimization, architectural level estimation & synthesis.

References:

1. Kaushik Roy, Sharat Prasad, *Low-Power CMOS VLSI Circuit Desig*n, Wiley, 2000
2. Gary K. Yeap, *Practical Low Power Digital VLSI Design*, KAP, 2002

3. Rabaey, Pedram, *Low power design methodologies*, Kluwer Academic, 1997

EC22305 RF IC Design **SECOND SEMESTER (E-IV)**

Introduction to RF design and wireless technology: design and applications, complexity and choice of technology, basic concepts in RF design: Nonlinearly and time variance, intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion. RF modulation, analog and digital modulation of RF circuits, comparison of various techniques for power efficiency, coherent and noncoherent detection, mobile RF communication and basics of multiple access techniques. receiver and transmitter architectures, direct conversion and two-step transmitters. RF Testing: RF testing for heterodyne, homodyne, image reject, direct IF and sub-sampled receivers, BJT and MOSFET behaviour at RF frequencies, modeling of the transistors and SPICE model, noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation, RF circuits design.

Overview of RF filter design, active RF components & modeling, matching and biasing networks, basic blocks in RF systems and their VLSI implementation, low noise amplifier design in various technologies, design of mixers at GHz frequency range, various mixers-working and implementation, Oscillators- basic topologies VCO and definition of phase noise, noise power and trade off, resonator VCO designs, quadrature and single sideband generators, radio frequency synthesizers- PLLs, various RF synthesizer architectures and frequency dividers, power amplifier design, liberalization techniques, design issues in integrated RF filters.

References:

1. Thomas H. Lee, *Design of CMOS RF Integrated Circuits*, Cambridge University press 1998
2. B. Razavi, *RF Microelectronics*, PHI, 1998
3. R. Jacob Baker, H.W. Li and D. E. Boyce, *CMOS Circiut Design, layout and Simulation*, PHI 1998
4. Y. P. Tsividis, *Mixed Analog and Digital Devices and Technology*, TMH 1996

Introduction to Embedded systems: Introduction, categorization of embedded systems, exemplary systems, selection of processor and memory for embedded systems, DMA, I/O devices, interrupt service handling for embedded systems, embedded tools in C/C++, memory optimization.

8-bit Microcontrollers: Introduction to MCS-51 family, architectural features, organization of data & program memories, orthogonal architectural features, addressing modes, instruction set, programming, 8051 interrupts, writing ISRs, SFRs, programming on-chip devices, UART and serial port programming, power saving modes.

Interfacing & Applications: External memory interfacing, interfacing ADC, display systems (7-Seg & LCDs)**,** potentiometer position measurements, temperature monitoring/control for ACs, light sensors for Robotics, ultrasonic sistance measurements, PWM motor control, RS-232 interface, servo positioning system.

Enhanced MCS-51 Features: Architectural enhancements in scratchpad RAM, Watchdog timers, onboard PWM, HSM controllers, high speed serial port, introduction to MCS—151/251.

Real Time Operating System: Introduction to OS concept, system services, RTOS basics, task scheduling, interrupt latency, example RTOS for MCS-51: RTOSLITE & FULLRTOS.

References:

1. Raj Kamal, *Embedded System Architecture, Programming and Design*, 2nd Ed, Tata McGraw Hill
2. Myke Predko, *Programming and Customizing the 8051 Microcontroller*, Tab Books/ Tata McGraw Hill
3. M. A. Mazidi, J.G. Mazidi and R. D. McKinlay, *The 8051 Microcontrollers and Embedded Systems: Using Assembly and C*, 2nd Ed, Pearson Education
4. John Catsoulis**,** *Designing Embedded Hardware*, O'Reilly Media, Inc
5. K. J. Ayala, *The 8051 Microcontrollers Architecture Programming & Applications*, 2nd Ed, Penram International
6. L. B. Das, *Embedded Systems: An Integrated Approach*, Pearson Education

EC22307 Mixed Mode Signal Processing **SECOND SEMESTER (E-V)**

Active & Passive elements: GIC, FDNR, NIC realizations, Immittance & Inductor Simulation, Deboo circuits & Riordan gyrators, current conveyors (CC^{+}& CC^{++}), FTFN & CFAs, generalized active RC realizations, Delyiannis-Friend circuits, Multiple VCVS & KHN realizations using CFAs, state variable & switched capacitor filters, relative sensitivity, Pole position & coefficient (Q, W_n) sensitivity, spread considerations.

Basic CMOS circuit techniques & current mode signal processing: Mixed-signal VLSI chips, basic CMOS circuits, basic gain stage, gain boosting techniques, super MOS transistor, MOS multipliers and resistors, Bipolar and low-voltage BiCMOS building block, continuous time signal processing, current mode low power neural networks signal processing blocks.

Mixed-signal circuits, nonlinear analog circuits, dynamic analog circuits, sampled-data analog filters, over sampled A/D converters, D/A converters and analog integrated sensors: First-order and second SC circuits, Bilinear transformations.

Digital tuning/Digital programmability: SPRA/SPCA (switched programmable resistor array & switched programmable capacitor array), m-DAC (Multiplier-DA converter) and their interfacing to microcontroller/micro computer system, digitally programmable active RC network using high speed analog/ mixed- signal building block.

References:

1. Mohammed Ismail & Terri Fiez, *Analog VLSI signal and Information Processing,* McGraw-Hill International Editions, 1994
2. Malcom R. Haskard & Lan C. May, *Analog VLSI Design- NMOS and CMOS*, Prentice Hall, 1998
3. Randall L Geiger, Phillip E. Allen & Noel K.Strader, *VLSI Design Techniques for Analog and Digital Circuits*, Mc Graw Hill International Company, 1990
4. Jose E. France & Yannis Tsividis, *Design of Analog-Digital VLSI Circuits for Telecommunication and Signal Processing*, Prentice Hall, 1994
5. C. Toumazou, F. J. Lidgey & D. G. Haigh, *Analog IC Design. The Current-Mode Approach,* Peter Peregrinus Ltd., 1990

EC22308 ASIC Design **SECOND SEMESTER (E-V)**

Types of ASICs, design flow, economics of ASICs, ASIC cell libraries, CMOS logic cell, data path logic cells, I/O cells, cell compilers.

ASIC Library design: Transistors as resistors, parasitic capacitance, logical effort, Programmable ASIC design software: design system, logic synthesis, half gate ASIC. Low level design entry: schematic entry, low level design languages, PLA tools, EDIF - an overview of VHDL and Verilog.

Logic synthesis in Verilog and VHDL simulation.

ASIC construction, floor planning & placement, routing.

References:

1. J.S. Smith, *Application specific Integrated Circuits,* Addison Wesley, 1997

EC22309 VLSI Testing and Testable Design **SECOND SEMESTER (E-V)**

The need for testing, the problems of digital and analog testing, design for test, software testing. Faults in Digital circuits: General introduction, controllability and observability. Fault models - stuck-at faults, bridging faults, intermittent faults.

Digital test pattern generation: Test pattern generation for combinational logic circuits, manual test pattern generation, automatic test pattern generation - Roth's D-algorithm, developments following Roth's D-algorithm, pseudo random test pattern generation, test pattern generation for sequential circuits, exhaustive, non-exhaustive and pseudo random 70 test pattern generation, delay fault testing.

Signatures and self test: Input compression Output compression arithmetic, Reed-Muller coefficients, spectral coefficients, coefficient test signatures, signature analysis and online self test.

Testability techniques: Partitioning and ad-hoc methods and scan-path testing, boundary scan and IEEE standard 1149.1, offline Built in Self Test (BIST), hardware description languages and test.

Testing of analog and digital circuits: testing techniques for filters, A/D converters, RAM, programmable logic devices and DSP.

References:

1. Stanley L. Hurst, *VLSI Testing: digital and mixed analogue digital techniques*, Pub: Inspec / IEE, 1999
2. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, *Testing & Testable Design*

EC22201 FPGA / CPLD Lab **SECOND SEMESTER (E-VI)**

List of experiments:

1. Design & simulation of AND, NAND, NOR, EX-OR, EX-NOR gate using Verilog HDL and VHDL
2. Design & simulation of half and full adder, half and full subtractor
3. Design & simulation of 4-bit parallel-adder
4. Design & simulation of full adder using half adder
5. Design & simulation of 4:1 multiplexer
6. Design & simulation of 16:1 multiplexer using 4:1 multiplexer
7. Design & simulation of 3:8 decoder
8. Design & simulation of D, T, SR, JK & master-slave Flip-Flops
9. Design & simulation of ring and Johnson-counters
10. Design & simulation of universal shift-register
11. Design & simulation of 3-bit Gray counter
12. Verify all the above experiments on FPGA kit

EC22202 Analog IC and Digital IC Design Lab **SECOND SEMESTER (E-VI)**

List of Experiments:

1. Design NOT, NOR, NAND gates using HSPICE & CADENCE and compute the delay between input and output waveforms
2. Design 2:1 MUX using HSPICE & CADENCE and compute the delay between input and output waveforms
3. Design XOR, NOR, NAND gates using HSPICE & CADENCE and compute the delay between input and output waveforms and compare the difference between CMOS and pseudo techniques
4. Design XOR gate using CMOS and pseudo techniques using HSPICE & CADENCE and compute the delay between input and output waveforms and compare them
5. Design and simulate D-Flip-flop as a Master–slave configuration using HSPICE & CADENCE
6. Design ring oscillator using HSPICE & CADENCE and compute the delay between input and output waveforms
7. Design 2:1 MUX using transmission gates using HSPICE & CADENCE

8. Design 6-T SRAM using HSPICE & CADENCE and compute the delay between input and output waveforms
9. Design and simulate CS-Amplifier and calculate transconductance using CADENCE
10. Design and simulate current mirror circuit and calculate transconductance using CADENCE
11. Design and simulate differential-amplifier circuit and calculate transconductance using CADENCE
12. Design and simulate Inverter circuit and calculate delay, power, for various values of W/L using CADENCE
13. Design and simulate Inverter, NAND, NOR circuits and calculate noise margin using HSPICE & CADENCE
14. Design and simulate Inverter, NAND, XOR circuits and calculate delay, power for pre-layout and post-layout using CADENCE

EC22203 Simulation Lab-II **SECOND SEMESTER (E-VI)**

List of Experiments:

1. Design and simulate n-channel bulk MOSFET of 1 μm gate length and extract its I-V characteristics using TCAD
2. Design and simulate n-channel SOI MOSFET of 1 μm gate length and extract its I-V characteristics using TCAD
3. Design and simulate n-channel UTB SOI MOSFET and extract its electrical performance characteristics using TCAD
4. Design and simulate n-channel double gate (DG) MOSFETs and extract their electrical performance characteristics using TCAD

5 Design and simulate p-channel double gate (DG) MOSFETs and extract their electrical performance characteristics using TCAD

6. Design and simulate n-channel double gate (DG) MOSFET and extract its analog performance parameters using TCAD

7 Design and simulate n-channel double gate (DG) MOSFET and extract its RF performance parameters using TCAD

8. Compare the electrical and analog performance parameters of short channel bulk and SOI MOSFETs using TCAD

9. Design and simulate a short channel bulk inverter circuit and extract its delay using TCAD
10. Design and simulate a short channel double gate (DG) inverter circuit and extract its delay using TCAD
11. Design and simulate a short channel triple gate (TG) inverter circuit and extract its delay using TCAD